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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,387	02/26/2004	Randy L. Yach	068354.1395	4790

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BAKER BOTTS L.L.P.
PATENT DEPARTMENT
98 SAN JACINTO BLVD., SUITE 1500
AUSTIN, TX 78701-4039

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,387	RANDY L. YACH	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8-10,12,15,17-21,23,25,27 and 28* is/are rejected.

7)☒ Claim(s) *4,5,7,11,13,14,16,22,24 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed February 26, 2004.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "**132**" has been used to designate both **integrated circuit substrate** and **P-well** on page 7, lines 9 and 14. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because "**comprises**" should have been **includes** in line 6, page 15. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 8-10, 12, 15, 17-21, 23, 25 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (6,060,752) in view of Cheng et al. (US 6,576,934 B2).

In regard to claim 1, Williams teaches an ESD-protection structure, comprising: an integrated circuit having a lighter doped p-silicon well (P- well) 902; a lighter doped n-silicon well (N- well) 904 in the P- well 902; a plurality of heavier doped p-silicon diffusions (P+ diffusions) 906 & 908 in the N- well 904; a first heavier doped n-silicon diffusion (N+ diffusion) in the N- well, wherein the first N+ diffusion surrounds the plurality of P+ diffusions 906 & 908; a second heavier doped n-silicon diffusion (N+ diffusion) 912 & 916 in the P- well 902, wherein the second N+ diffusion 916 surrounds the first N+ diffusion; a bond pad 918 & 924 connected to the plurality of P+ diffusions 906 & 908; and a connection to the second N+ diffusion 912 & 916 (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claim 18, Williams teaches an ESD-protection structure, comprising: an integrated circuit having a lighter doped p-silicon well (P- well) 902; a lighter doped n-silicon well (N- well) 904 in the P- well 902; a plurality of heavier doped p-silicon diffusions (P+ diffusions) 906 & 908 in the N- well 904; a first heavier doped n-silicon diffusion (N+ diffusion) in the N- well, wherein the first N+ diffusion surrounds the

plurality of P+ diffusions 906 & 908; a second heavier doped n-silicon diffusion (N+ diffusion) 912 & 916 in the P- well 902, wherein the second N+ diffusion 916 surrounds the first N+ diffusion; a field oxide FOX located between the first and second N+ diffusions; a bond pad 918 & 924 connected to the plurality of P+ diffusions 906 & 908; and a connection to the second N+ diffusion 912 & 916 (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claim 28, Williams teaches a system for protecting an integrated circuit from ESD damage, the system comprising: an ESD-protection structure for at lest one of a plurality of input and output connections of an integrated circuit, wherein the ESD-protection structure comprises: an integrated circuit having a lighter doped p-silicon well (P- well) 902; a lighter doped n-silicon well (N- well) 904 in the P- well 902; a plurality of heavier doped p-silicon diffusions (P+ diffusions) 906 & 908 in the N- well 904; a first heavier doped n-silicon diffusion (N+ diffusion) in the N- well, wherein the first N+ diffusion surrounds the plurality of P+ diffusions 906 & 908; a second heavier doped n-silicon diffusion (N+ diffusion) 912 & 916 in the P- well 902, wherein the second N+ diffusion 916 surrounds the first N+ diffusion; a bond pad 918 & 924 connected to the plurality of P+ diffusions 906 & 908; and a connection to the second N+ diffusion 912 & 916 (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

However, Williams fails to teach the first N+ diffusion overlapping the N- well into the P- well and the P-well being an integrated circuit substrate.

Cheng et al. teach a first N+ diffusion 624 overlapping the N- well into the P- well 21 and the P-well 21 being an integrated circuit substrate (Figure 6, column 4, lines 1-62).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ESD-protection structure as taught by Williams with the ESD-protection structure having a first N+ diffusion overlapping the N-well into the P- well and a P-well being an integrated circuit substrate as taught by Cheng et al. to provide an ESD-protection device with a very low holding voltage (column 1, lines 34-37).

In regard to claim 2, Cheng et al. teach the P- well 21 being the integrate circuit substrate (Figure 6, column 4, lines 1-62).

In regard to claim 3, Williams teaches a field oxide FOX located between the first and second N+ diffusions (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claim 6, Cheng et al. teach the plurality of P+ diffusions 622 being rectangular shaped (Figure 6, column 4, lines 1-62).

In regard to claims 8, 19 and 21, Williams teaches the bond pad 918 & 924 connected to the plurality of P+ diffusions 606 & 908 with a first plurality of conductive vias (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regards to claim 9, 20 and 23, Williams teaches the connection to the second N+ diffusions 912 & 916 being with a second plurality of conductive vias (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claim 10, Williams teaches the first plurality of conductive vias being metal (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claim 12, Williams teaches the second plurality of conductive vias being metal (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

In regard to claims 15 and 25, Cheng et al. teach the P- well 21 coupled to ground 39 (Figure 6, column 4, lines 1-62).

In regard to claims 17 and 27, Williams teaches the plurality of P+ diffusions 906 & 908, the first N+ diffusions and the N- well 904 located substantially under the bond pad 918 & 924 (Figure 9A, columns 6-7, lines 53-67 and 1-63, respectively).

Allowable Subject Matter

Claims 4-5, 7, 11, 13-14, 16, 22, 24 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to ESD-protection structures:

Brodsky et al. (US 2004/0217425 A1) Chen et al. (5,166,089)

Fukuda (US 6,215,157 B1) Harrington, III et al. (5,181,091)

Horiguchi (5,932,914) Huang et al. (US 6,441,439 B1)

Reddy et al. (US 2004/0251502 A1) Wei et al. (5,719,733)

Zhang (US 2005/0045909 A1) Zitouni et al. (US 2004/0045909 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
July 25, 2005

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